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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	SHIMOKAWA, et al.
Serial No.:	09/972,178
Filed:	October 9, 2001
For:	PB-FREE SOLDER-CONNECTED STRUCTURE AND ELECTRONIC DEVICE
Group:	1775
Examiner:	J. Zimmerman

DECLARATION UNDER 37 CFR 1.132

I, Masahide OKAMOTO, a citizen of Japan, residing at 29-3-410, Yayoidai, Izumi-ku, Yokohama 245-0008, Japan, DECLARE THAT:

1. I graduated from the Faculty of Chemical Engineering at Tokyo Institute of Technology in March, 1984, and from the master's course thereof in March, 1986.

2. I am presently employed by Hitachi, Ltd., and have been so employed since April, 1986.

3. After entering Hitachi, Ltd., at Hitachi Research Laboratory, I was engaged in research/development on ceramic materials and process technologies for computer packaging.

4. Thereafter, I was transferred to Production Engineering Research Laboratory of Hitachi, Ltd., where I was a leader of a lead-free soldering group from 2000 to 2002. I have been engaged in development of lead-free soldering technologies for Hitachi, Ltd., and affiliated companies.

5. I have also promoted an IMS (Intelligent Manufacturing Systems) EFSOT (Next Generation Environment-Friendly Soldering Technology) project as an Inter-regional coordinator and a Japanese regional coordinator from 2000 until now.

Presentations and Publications

6. I have given a presentation at the Japan Symposium of EcoDESIGN 2002, held in December, 2002, the title of which presentation was "Consideration on reliability of lead-joints with utilization of Pb-free solder".

7. I have given a presentation at the Second International Symposium on Environmentally Conscious Design and Inverse Manufacturing of EcoDESIGN 2001, held in December, 2001, the title of which presentation was "Reliability of joints between Pb-free solder and Pb-free metallized leads".

8. I had a report published in the scholarly journal (Vol. 3, No. 7 (2000)) of the Japan Institute of Electronics Packaging, the title of which is "Founding of EFSOT of IMS project, and Summary thereof".

9. I have given a presentation at the American Ceramic Society, 96th Annual Meeting & Exposition held in May, 1994, the title of which presentation was "Glass Ceramics/Al203 Filler Composites for Low-temperature Sintered Substrates".

10. I have given a presentation at IMC 1990, the 6th International Microelectronics Conference, held in May, 1990, the title of which presentation was "AIN Application for PGA Package".

11. I had a report published in the scholarly journal (Vol. 97, pp. 1486-1493 (1989)) of the Japan Ceramic Society, the title of which is "Effect of Microstructure on Thermal Conductivity of AIN Ceramics".

Patent Applications/Patents

12. I am an inventor named in the following patent applications or patents in the U.S.A. and/or in Japan:

(a) Title of Invention: "Packaging method using lead-free solder", U.S. App. No. 09/929,215 (filed on August 13, 2001), based on JP Pat. Appln. No. 2001-233627 (filed on August 1, 2001).

(b) Title of Invention: "Wave soldering method using lead-free solder, Apparatus therefor, and Wave-soldering assembly", U.S. Appln. No. 10/133,778 (filed on April 25, 2002), based on JP Pat. Appln. No. 2001-388814 (filed on December 21, 2001).

(c) Title of Invention: "Circuit substrate and Electronics computer, using sintered glass ceramics", U.S. Patent No. 5,825,632 (issued October 20, 1998), based on JP Pat. Appln. No. 06-195806 (filed August 19, 1994).

(d) Title of Invention: "Electronic device with lead-free solder joints", JP Pat. Appln. No. 2000-180713 (filed on June 12, 2000).

(e) Title of Invention: "Circuit substrate, Manufacturing method therefor, Electronic device package, and Green sheet", JP Pat. Appln. No. 06-318487 (filed on December 21, 1994).

Experimentation Performed

13. The following experimentation was performed in order to determine differences between (1) a soldered structure formed by plating only a single layer of Sn-Bi (having a thickness of 10 μm) on the lead of a semiconductor device prior to reflow-soldering (that is, an "S"-type electrode structure, having a layer of Sn-Bi, as

a surface layer, directly in contact with the lead), and (2) a soldered structure formed by plating two layers, of an outer Sn-2Bi layer (having a thickness of 4 μm) and an inner Sn layer (having a thickness of 6 μm), on the lead of a semiconductor device prior to reflow-soldering (that is, a "T"-type electrode structure).

14. The T-type electrode structure corresponds to that disclosed in U.S. Patent No. 6,110,608 to Tanimoto, et al., having two layers, of first and second plating layers, formed on the lead prior to reflow-soldering, the second plating layer having a lower melting point than that of the first plating layer.

15. Specifically, the following were prepared:

(a) Invention specimen: A single layer of Sn-Bi was provided on a lead of 42 alloy, of a QFP Package, by electroplating, to form the single layer described in Item 13(1) herein. The electroplating of Sn-Bi was conducted by the conventional way in Production Engineering Research Laboratory of Hitachi, Ltd. with utilization of a commercially available plating solution provided from UEMURA KOHGYO K.K.

(b) Comparative specimen (corresponding U.S. Patent No. 6,110,608 to Tanimoto, et al.,): Double layers of Sn and Sn-2Bi were provided on a lead of 42 alloy, of a QFP package, by electroplating, to form the two layers described in Item 13(2) herein. A first electroplating layer of Sn was formed on the lead in K.K. NISHIHARA RIKOH and the thus plated intermediate product was provided to Hitachi, Ltd. Thereafter, the electroplating of Sn-2Bi was conducted by the conventional way in Production Engineering Research Laboratory of Hitachi, Ltd. with utilization of a commercially available plating solution provided from UEMURA KOHGYO K.K. In the electroplating, the chemical composition of the Sn-2Bi plating

layer was controlled by selecting a type of the plating solution and suitable plating conditions.

(c) Printed circuit boards with Cu pads were prepared. A solder paste of Sn-2. 8Ag-15Bi was provided on the Cu pads by the screen printing method.

16. Specimens as prepared in Item 15(a) and Item 15(b) were positioned on respective printed circuit boards prepared as in Item 15(c), with the leads positioned on the Cu pads. Resulting structure was then heated up to a temperature of 220℃ and kept at the temperature for 10 seconds in the atmosphere in order to conduct reflow-soldering.

17. After conducting the reflow-soldering to form solder joints, a tractive force was applied to the QFP package to fracture the solder joints. The fractured surfaces of a lead side and a board side were observed by means of an electron microscope. Presence of elements at the fractured surfaces were identified by means of EDX (Energy Dispersive X-ray Spectroscopy).

*Note: The experimentation was carried out by H. SHIMOKAWA who is one of the inventors of the present application. However, she is now suspended from office because of her childbirth. Therefore, I, Masahide OKAMOTO, declare herein on her behalf, who is a supervisor of the lead-free soldering group in which she was engaged and who is familiar with lead-free soldering technologies as aforementioned.

Results and Conclusions

18. Four photographs are attached hereto as Figure 1, each of which shows a state of fracture of a surface of a solder joint after a lead was drawn apart from the

solder joint which was formed by reflow-soldering of a lead structure (S- or T-type) on Cu pads of printed circuit boards, as described in Item 16. The photographs include observations of a lead side and a substrate electrode side.

19. From the photographs, it can be seen that the Bi-phase is uniformly dispersed in the fracture surface of the solder joint (both of the lead side and the substrate electrode side) in the case of using the lead structure with a single layer of Sn-1Bi (Bi dispersion is homogeneous), and that the Bi-phase is not uniformly dispersed in the fracture surface of the solder joint (both of the lead side and the substrate electrode side) in the case of using the lead structure with two layers of the Sn-2Bi layer and the Sn layer (Bi dispersion is heterogeneous).

20. Taking into consideration that, in solder joints, cracks or a fracture (or separation) of a lead is liable to occur at an agglomeration site of Bi, it can be easily understood that the solder joint formed with utilization of the S-type electrode structure has a higher reliability in bonding than the solder joint formed with utilization of the T-type electrode structure.

21. Further, the solder joint formed with utilization of the T-type electrode structure (having two layers, of Sn-2Bi and Sn) is not stable over time because the Bi dispersion is heterogeneous. In contrast, the solder joint formed with utilization of the S-type electrode structure (having a single layer of Sn-1Bi) is stable over time because the Bi dispersion is homogeneous.

22. As will be apparent from the test result, in electronic devices a solder joint according to the present invention with utilization of the lead provided with a single layer of Sn-Bi prior to reflow-soldering is excellent in reliability in bonding and stable

over time in comparison with a solder joint with utilization of the lead provided with two layers prior to reflow-soldering, corresponding to Tanimoto, et al.

23. It should be also noted that, in fabrication processes of electronic devices, a single plating process for a single plating layer, for leads of semiconductor devices, is more advantageous as compared with double plating processes for two plating layers, for leads of semiconductor devices, in the viewpoint of saving a production cost and improvement of productivity.

The undersigned Declarant declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 9th day of June, 2003

Masahide Okamoto

Masahide OKAMOTO